REMARKS

Pursuant to the present amendment, claims 1, 3, 9 and 11 have been amended and claims 2, 4-5, 10 and 16-20 have been canceled. Thus, claims 1, 3, 6-9, 11-15 and 21-22 are pending in the present application. No new matter has been introduced by way of the present amendment. Reconsideration of the application is respectfully requested.

In the Office Action, claims 1-22 were rejected under 35 U.S.C. § 102 as allegedly being anticipated by Cappelletti (U.S. Patent No. 5,793,675). Applicants respectfully traverse the Examiner's rejections.

As the Examiner well knows, an anticipating reference by definition must disclose every limitation of the rejected claim in the same relationship to one another as set forth in the claim. *In re Bond*, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). To the extent the Examiner relies on principles of inherency in making the anticipation rejections in the Office Action, inherency requires that the asserted proposition necessarily flow from the disclosure. *In re Oelrich*, 212 U.S.P.Q. 323, 326 (C.C.P.A. 1981); *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1463-64 (Bd. Pat. App. & Int. 1990); *Ex parte Skinner*, 2 U.S.P.Q.2d 1788, 1789 (Bd. Pat. App. & Int. 1987); *In re King*, 231 U.S.P.Q. 136, 138 (Fed. Cir. 1986). It is not enough that a reference could have, should have, or would have been used as the claimed invention. "The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Oelrich*, at 326, quoting *Hansgirg v. Kemmer*, 40 U.S.P.Q. 665, 667 (C.C.P.A. 1939); *In re Rijckaert*, 28 U.S.P.Q.2d 1955, 1957 (Fed. Cir. 1993), quoting *Oelrich*, at 326; see also *Skinner*, at 1789. "Inherency ... may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Skinner*, at 1789, citing *Oelrich*. Where anticipation is found through inherency, the Office's burden of establishing prima facie anticipation includes the burden of providing "...some evidence or scientific reasoning to

establish the reasonableness of the examiner's belief that the functional limitation is an inherent characteristic of the prior art." *Skinner* at 1789.

Moreover, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. Moreover, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988); M.P.E.P. § 2143.03.

With respect to alleged obviousness, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Health-care Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. The consistent criterion for determining obviousness is whether the prior art would have suggested to one of ordinary skill in the art that the process should be carried out and would have a reasonable likelihood of success, viewed in the light of the prior art. Both the

suggestion and the expectation of success must be founded in the prior art, not in the Applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991; *In re O'Farrell*, 853 F.2d 894 (Fed. Cir. 1988); M.P.E.P. § 2142.

Pursuant to the present amendment, independent claim 1 has been amended to recite that the semiconductor device is a flash memory device and that the electrical test is performed to determine a duration of a programming cycle for the flash memory device. Claim 1 has been further amended to recite that the act of determining at least one parameter of a process operation to be performed to form a gate insulation layer on a subsequently formed flash memory device is based upon the determined duration of the programming cycle.

Independent claim 9 has been amended in a similar fashion as set forth above with respect to claim 1 except that the electrical test is performed to determine the duration of an erase cycle for the flash memory device.

As thus amended, it is respectfully submitted that all pending claims are in condition for immediate allowance.

Cappelletti is understood to be directed to evaluating the quality of gate oxide layers employed in various memory devices. Abstract. In the test structure disclosed therein, all of the cells are connected electrically parallel to one another. Col. 2, l. 64 – Col. 3, l. 12. The structure disclosed therein is electrically stressed in such a manner so as to extract electrons from the floating gate of defective gate oxide cells while the other non-defective cells remain unchanged. Col. 3, ll. 30-46. Cappelletti even discloses stressing the test structure disclosed therein in ramped stages. Col. 4, l. 66 – Col. 5, l. 26. After all the testing is done, if the difference between resulting VRL and VRH values exceeds a preselected threshold, the structure is considered defective. Col. 5, ll. 32-35.

With this understanding of Cappelletti, it is respectfully submitted that Cappelletti does not anticipate nor render obvious any of the pending claims. Specifically, it is respectfully submitted that, although Cappelletti does disclose performing various electrical tests on a test structure to determine the quality of a gate oxide layer, at no point does Cappelletti disclose nor suggest performing at least one electrical test to determine the duration of a programming cycle of a flash memory device or to determine the duration of an erase cycle for a flash memory device. At worst, in the test structure described in Cappelletti, it is not clear that the a programming cycle or an erase cycle can even be performed on the test structure. While Cappelletti does disclose that the structure 10 may be subjected to a UV erase procedure, that is not an erase cycle as that phrase is employed and used in the specification. A plain reading of the specification reflects that the erase cycle disclosed therein is an electrically controlled erasure of the flash memory device. While the cells of the test structure 10 disclosed in Cappelletti are electrically connected parallel to one another, it is not clear that the structure described therein is capable of performing a test to determine the duration of a programming cycle, or the duration of an erase cycle. Simply put, there does not appear to be any associated circuitry with the test structure that would enable the memory cells described therein to be programmed or electrically erased. Thus, it is respectfully submitted that, for a variety of reasons, the structure in Cappelletti does not disclose the inventions set forth in the pending claims.

Moreover, it is respectfully submitted that Cappelletti does not render the pending claims obvious. While Cappelletti does disclose a test structure for determining the quality of various gate oxide layers, at no point does it even remotely suggest performing an electrical test to determine the duration of a programming cycle for a flash memory device or to determine the erase cycle for a flash memory device. Moreover, Cappelletti does not disclose determining at least one parameter of a process operation to be performed to form a gate insulation layer on a

subsequently manufactured device based upon this determined programming cycle or erase cycle as set forth in the various claims set forth in the application.

A recent Federal Circuit case makes it crystal clear that, in an obviousness situation, the prior art must disclose each and every element of the claimed invention, and that any motivation to combine or modify the prior art must be based upon a suggestion in the prior art. *In re Lee*, 61 U.S.P.Q.2d 143 (Fed. Cir. 2002). Conclusory statements regarding common knowledge and common sense are insufficient to support a finding of obviousness. *Id.* at 1434-35. It is respectfully submitted that any attempt to assert that the amended claims currently pending in the application would have been obvious in view of Cappelletti or any other art of record is necessarily based upon an improper use of hindsight using Applicants' disclosure as a roadmap.

Although Cappelletti does disclose performing electrical tests on the test structure disclosed therein to determine various characteristics of a gate oxide layer, at no point does Cappelletti disclose or suggest determining ultimate performance characteristics of a memory device, *e.g.*, the duration of a programming cycle or the duration of an erase cycle, as set forth in the pending claims. Simply put, the pending claims involve determining an ultimate performance characteristic of a memory device, and, based upon that ultimate performance characteristic, determining a parameter of a process operation to be performed to form a gate insulation layer on a subsequently formed memory device. Of course, the Examiner will need to consult the exact language of each pending claim to determine all limitations set forth therein. By using the duration of the programming cycle and the duration of the erase cycle to determine processing parameters for the formation of gate insulation layers on subsequently formed memory devices, the production of memory devices that meet ultimate performance specifications can be improved.

For at least the aforementioned reasons, it is respectfully submitted that all pending claims are in condition for immediate allowance. The Examiner is invited to contact the undersigned attorney at (713) 934-4055 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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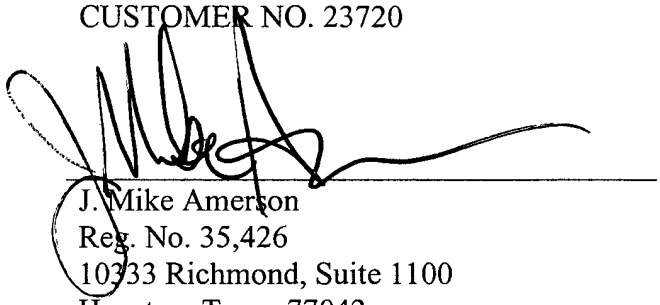

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